IN THE CLAIMS

Please amend claims 1-13, 17, 18-28, and 33-53 as follows:

1. (CURRENTLY AMENDED) A[[n]] [[adder]] circuit for adding a signal at a first input *(A)* and a second input *(B)* to produce a[[n]] [[adder]] sum output *(S)* according to a bypass signal, comprising:

a ~~bypass~~ third input (*bypass*) for accepting the bypass signal; and

a logic circuit, communicatively coupled to the ~~bypass~~ third input (*bypass*) and at least one of the first input *(A)* and the second input *(B)*, the logic circuit configured to hold at least one of a value of the first input *(A)* and a value of the second input *(B)* according to the ~~bypass~~ third input (*bypass*)[[.]] ; and

a bypass path through which at least one of the first input *(A)* and the second input *(B)* is routed according to the bypass signal;

a second logic circuit communicatively coupled to the third input *(bypass)* and an adder output and an output of the bypass path, the second logic circuit configured to pass only one of the adder output and an output of the bypass path to the sum output (S) according to the third input *(bypass)*.

2. (CURRENTLY AMENDED) The [[adder]] circuit of claim 1, wherein the logic circuit further generates the [[adder]] sum output *(S)* without computing a new [[adder]] sum output *(S)* according to the ~~bypass~~ third input (*bypass*).

3. (CURRENTLY AMENDED) The [[adder]] circuit of claim 1, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the logic circuit further holds a value of the carry input *(C)* according to the ~~bypass~~ third input (*bypass*).

4. (CURRENTLY AMENDED) The [[adder]] circuit of claim 1, wherein the logic circuit further generates a carry output *(CARRY)* without computing a new adder output according to the bypass signal (*bypass*).

5. (CURRENTLY AMENDED) The [[adder]]] circuit of claim 1, wherein the logic circuit comprises a transmission gate adder.

6. (CURRENTLY AMENDED) The [[adder]] circuit of claim 5, wherein the transmission gate adder comprises:

a first multiplexer having a first multiplexer first input communicatively coupled to the first input *(A)*, a first multiplexer second input, and a first multiplexer control input;

a second multiplexer having a second multiplexer first input communicatively coupled to the second input *(B)*, a second multiplexer second input, and a second multiplexer control input;

a first logic module having a first logic module first input, a first logic module second input, and a first logic module output, the first logic module output having an EXCLUSIVE OR relationship between the first logic module first input and the first logic module second input; and

wherein the first logic module input is communicatively coupled to the first input *(A)*, the logic module second input is communicatively coupled to the second input *(B)*, and the first logic module output is communicatively coupled to the first multiplexer control input and the second multiplexer control input.

7. (CURRENTLY AMENDED) The [[adder]] circuit of claim 6, wherein the first logic module is an EXCLUSIVE OR gate.

8. (CURRENTLY AMENDED) The [adder]] circuit of claim 7, further comprising:

a first inverter communicatively coupled between the first input *(A)* and the first multiplexer first input; and

a second inverter communicatively coupled between the second input *(B)* and second multiplexer first input.

9. (CURRENTLY AMENDED) The [adder]] circuit of claim 1, wherein the logic circuit is configured to hold the value of the first input *(A)* and the value of the second input *(B)* according to the ~~bypass~~ third input (*bypass*).

10. (CURRENTLY AMENDED) The [adder]] circuit of claim 9, wherein the logic circuit comprises a transmission gate adder.

11. (CURRENTLY AMENDED) The [adder]] circuit of claim 10, wherein the transmission gate adder comprises:

a first multiplexer having a first multiplexer first input communicatively coupled to the first input *(A)*, a first multiplexer second input, and a first multiplexer control input;

a second multiplexer having a second multiplexer first input communicatively coupled to the second input *(B)*, a second multiplexer second input, and a second multiplexer control input;

a first logic module having a first logic module first input, a first logic module second input, and a first logic module output, the first logic module output having an EXCLUSIVE OR relationship between the first logic module first input and the first logic module second input; and

wherein the first logic module input is communicatively coupled to the first input *(A)*, the logic module second input is communicatively coupled to the second input *(B)*, and the first logic module output is communicatively coupled to the first multiplexer control input and the second multiplexer control input.

12. (CURRENTLY AMENDED) The [[adder]] circuit of claim 6, wherein the logic circuit comprises:

a second logic module having a second logic module first input, a second logic module second input, and a second logic module output, the second logic module output having an EXCLUSIVE OR relationship between the second logic module first input and the second logic module second input; and

wherein the second logic module first input is communicatively coupled to the first logic module output.

13. (CURRENTLY AMENDED) The [adder]] circuit of claim 12, wherein the second logic module is an EXCLUSIVE OR gate.

14. (ORIGINAL) A device for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising

a bypass input (*bypass*); and

a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

15. (PREVIOUSLY PRESENTED) The device of claim 14, wherein the logic circuit is further configured to hold a value of at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

16. (PREVIOUSLY PRESENTED) The device of claim 14, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the logic circuit further holds a value of the carry input (*C*) according to the bypass input (*bypass*).

17. (CURRENTLY AMENDED) The device of claim 14, wherein the logic circuit further regenerates a carry output *(CARRY)* without computing a new adder output according to the bypass [[signal]] input (*bypass*).

18. (CURRENTLY AMENDED) A[[n]] ~~adder~~ circuit for adding a signal at a first input *(A)* and a second input *(B)* to produce a[[n]] [[adder]] sum output *(S)* according to a bypass signal, comprising:

a ~~bypass~~ third input (*bypass*) for accepting the bypass signal; and

a holding means for holding a value of at least one of the first input *(A)* and the second input *(B)* according to the ~~bypass~~ third input (*bypass*); and

wherein the holding means is communicatively coupled to the ~~bypass~~ third input (*bypass*), the at least one of the first input *(A)* and the second input *(B)*, the holding means configured to hold at least one of a value of the first input *(A)* and a value of the second input *(B)* according to the ~~bypass~~ third input (*bypass*)[[.]] ;

a bypass path through which at least one of the first input *(A)* and the second input *(B)* are routed according to the bypass signal; and

a logic circuit communicatively coupled to the third input *(bypass)* and an adder output and an output of the bypass path, the logic circuit configured to pass only one of the adder output and the output of the bypass path to the sum output *(S)* according to the third input *(bypass)*.

19. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 18, wherein the holding means further comprises means for generating the adder output *(S)* without computing a new [[adder]] sum output according to the ~~bypass~~ third input (*bypass*).

20. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 18, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the holding means further holds a value of the carry input (*C*) according to the ~~bypass~~ third input (*bypass*).

21. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 18, wherein the holding means further generates the carry output *(CARRY)* without computing a new output according to the ~~bypass signal~~ third input (*bypass*).

22. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 21, wherein the holding means comprises a transmission gate adder.

23. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 22, wherein the transmission gate adder comprises:

a first multiplexing means having a first multiplexing means first input communicatively coupled to the first input *(A)*, a first multiplexing means second input, and a first multiplexing means control input;

a second multiplexing means having a second multiplexing means first input communicatively coupled to the second input *(B)*, a second multiplexing means second input, and a second multiplexing means control input;

a first logic means having a first logic means first input, a first logic means second input, and a first logic means output, the first logic means output having an EXCLUSIVE OR relationship between the first logic means first input and the first logic means second input; and

wherein the first logic means input is communicatively coupled to the first input *(A)*, the first logic means second input is communicatively coupled to the second input *(B)*, and the first logic means output is communicatively coupled to the first multiplexing means control input and the second multiplexing means control input.

24. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 23, further comprising:

a first inverting means communicatively coupled between the first input *(A)* and the first multiplexing means first input; and

a second inverter communicatively coupled between the second input *(B)* and second multiplexing means first input.

25. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 18, wherein the holding means is configured to hold a value of the first input *(A)* and a value of the second input *(B)* according to the ~~bypass~~ third input (*bypass*).

26. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 25, wherein the holding means comprises a transmission gate adder.

27. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 26, wherein the transmission gate adder comprises:

a first multiplexing means having a first multiplexing means first input communicatively coupled to the first input *(A)*, a first multiplexing means second input, and a first multiplexing means control input;

a second multiplexing means having a second multiplexing means first input communicatively coupled to the second input *(B)*, a second multiplexing means second input, and a second multiplexing means control input;

a first logic means having a first logic means first input, a first logic means second input, and a first logic means output, the first logic means output having an EXCLUSIVE OR relationship between the first logic means first input and the first logic means second input; and

wherein the first logic means input is communicatively coupled to the first input *(A)*, the logic means second input is communicatively coupled to the second input *(B)*, and the first logic means output is communicatively coupled to the first multiplexing means control input and the second multiplexing means control input.

28. (CURRENTLY AMENDED) The ~~adder~~ circuit of claim 27, wherein the logic means comprises:

a second logic means having a second logic means first input, a second logic means second input, and a second logic means output, the second logic means output having a relationship selected from a group comprising an EXCLUSIVE OR relationship and a multiplexing relationship between the second logic means first input and the second logic means second input; and

wherein the second logic means first input is communicatively coupled to the first logic means output.

29. (ORIGINAL) A device for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising:

a bypass input (*bypass*); and

a generating means, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the generating means configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

30. (PREVIOUSLY PRESENTED) The device of claim 29, wherein the generating means is further configured to hold a value of at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

31. (ORIGINAL) The device of claim 29, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the generating means further holds the carry input (*C*)according to the bypass input (*bypass*).

32. (PREVIOUSLY PRESENTED) The device of claim 29, wherein the generating means further generates a carry output *(CARRY)* without computing a new output according to the bypass signal (*bypass*).

33. (CURRENTLY AMENDED) A method of adding a signal at a first input *(A)* and a second input *(B)* to produce a[[n]] [[adder]] sum output *(S)*, comprising the steps of:

accepting a ~~bypass~~ third input (*bypass*); and

holding at least one of a value of the first input *(A)* and a value of the second input *(B)* and passing only one of an adder output and a routed at least one of the first input (A) and the second input (B) to the sum output *(S)* according to the ~~bypass~~ third input (*bypass*).

34. (CURRENTLY AMENDED) The method of claim 33, further comprising the step of generating the [[adder]] sum output without computing a new adder output according to the bypass input (*bypass*).

35. (CURRENTLY AMENDED) The method of claim 33, further comprising the step of:

holding a value of a carry input *(C)* according to the ~~bypass~~ third input (*bypass*).

36. (CURRENTLY AMENDED) The method of claim 33, further comprising the step of:

generating the carry output *(CARRY)* without computing a new output according to the ~~bypass signal~~ third input (*bypass*).

37. (CURRENTLY AMENDED) A [[logic]] circuit ~~that maps~~ having one or more inputs $A, B, \cdots$ ~~to~~ and ~~produce~~ producing one or more outputs $S1, S2, \cdots$ according to a mapping function mapping the inputs $A, B, \cdots$ to one or more mapper outputs, the circuit comprising:

a ~~bypass~~ further input *(bypass)*; and

a first [[logic]] circuit element communicatively coupled to the ~~bypass~~ further input *(bypass)*;

a second [[logic]] circuit element, communicatively coupled to at least one of the inputs $A, B, \cdots$ that conditionally holds a value of one of the inputs $A, B, \cdots$ according to the ~~bypass~~ further input *(bypass)*[[.]] ;

a bypass path through which one or more of the inputs $A, B, \cdots$ are routed according to the further input *(bypass)*;

a third circuit element, communicatively coupled to the further input *(bypass)* and the one or more mapper outputs and an output of the bypass path, the third circuit element configured to pass only one of the (1) one or more mapper outputs and (2) output of the bypass path, according to the further input *(bypass)*.

38. (CURRENTLY AMENDED) The [[logic]] circuit of claim 37, wherein the mapping function is describable by a truth table.

39. (CURRENTLY AMENDED) The [[logic]] circuit of claim 38, wherein the [[logic]] circuit is an adder that adds the one or more inputs $A, B, \cdots$ to produce the one or more outputs $S1, S2, \cdots$.

40. (CURRENTLY AMENDED) The [[logic]] circuit of claim 37, wherein the [[logic]] circuit further generates at least one of the outputs $S1, S2, \cdots$ without computing a new output $S1, S2, \cdots$ according to the bypass input.

41. (CURRENTLY AMENDED) The [[logic]] circuit of claim 37, wherein the [[logic]] circuit holds a value of more than one of the inputs $A, B, \cdots$ according to the bypass input.

42. (CURRENTLY AMENDED) The [[logic]] circuit of claim 37, wherein the [[logic]] circuit is an adder and the [[logic]] circuit further comprises:

a carry input and a carry output; and

wherein the [[logic]] circuit further holds a value of the carry input according to the bypass input.

43. (CURRENTLY AMENDED) The [[logic]] circuit of claim 42, wherein the [[logic]] circuit further regenerates the carry input according to the bypass input.

44. (CURRENTLY AMENDED) The [[logic]] circuit of claim 37, wherein the second [[logic]] circuit element comprises at least one latch communicatively coupled to at least one of the inputs $A, B, \cdots$, wherein the latch includes a logical input, a clock input communicatively coupled to the bypass input, and an output, and the latch presents the logical input to the output only in response to a signal at the clock input.

45. (CURRENTLY AMENDED) A method of ~~mapping~~ processing one or more inputs $A, B, \cdots$ to produce one or more outputs $S1, S2, \cdots$ according to a mapping function having one or more inputs $A, B, \cdots$ and one or more mapper outputs, comprising the steps of:

accepting a ~~bypass~~ further input *(bypass)*; and

conditionally holding a value of one of the inputs $A, B, \cdots$ and passing only one of (1) the one or more mapper outputs and (2) an output of a bypass path through which one of the inputs $A, B, \cdots$ are routed to the one or more outputs $S1, S2, \cdots$ according to the ~~bypass~~ further input *(bypass)*.

46. (CURRENTLY AMENDED) The method of claim 45, further comprising the step of:

generating at least one of the outputs $S1, S2, \cdots$ without computing a new output $S1, S2, \cdots$ according to the ~~bypass~~ further input.

47. (CURRENTLY AMENDED) The method of claim 46, further comprising the step of generating at least another of the outputs $S1, S2, \cdots$ without computing a new another output $S1, S2, \cdots$ according to the ~~bypass~~ further input.

48. (CURRENTLY AMENDED) The method of claim 45, further comprising the step of:

holding a value of at least a second one of the inputs $A, B, \cdots$ according to the ~~bypass~~ further input.

49. (CURRENTLY AMENDED) The [[adder]] circuit of claim 1, wherein the logic circuit comprises an adder and at least one latch.

50. (CURRENTLY AMENDED) The device of claim 15, wherein the logic circuit comprises a latch.

51. (CURRENTLY AMENDED) The [[adder]] circuit of claim 18, wherein the holding means comprises a latch.

52. (CURRENTLY AMENDED) The method of claim 33, wherein the at least one of the value of the first input *(A)* and the value of the second input *(B)* is held according to the bypass input (*bypass*) by a latch having a clock input controlled by the ~~bypass~~ third input.

53. (PREVIOUSLY PRESENTED) The method of claim 45, wherein the value of one of the inputs $A, B, \cdots$ is conditionally held according to the ~~bypass~~ further input ~~is conditionally held~~ by a latch having a clock input controlled by the ~~bypass~~ further input.